CSPC2005 COMPUTER ORGANIZATION AND ARCHITECTURE (3-0-0)

Objectives of the course:

To expose the students to the following:

1. How Computer Systems work & the basic principles
2. Instruction Level Architecture and Instruction Execution
3. The current state of art in memory system design
4. How I/O devices are accessed and its principles.
5. To provide the knowledge on Instruction Level Parallelism
6. To impart the knowledge on micro programming
7. Concepts of advanced pipelining techniques.

Module-I: (8 Hrs.)

Functional blocks of a computer: CPU, memory, input-output subsystems, control Unit, Overview of Computer Architecture and Organization: Fundamentals of computer architecture, Organization of Von Neumann machine, Basic operation concepts, Performance and Historical perspective, Instruction set architecture of a CPU–registers, instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.

Module-II: (08 Hrs.)

Data representation: signed number representation, fixed and floating point representations, character representation. Computer arithmetic – integer addition and subtraction, ripple carry adder, carry look-ahead adder, etc. multiplication – shift and add, Booth multiplier, carry save multiplier, etc. Division restoring and non-restoring techniques, floating point arithmetic.

Module-III: (12 Hrs.)

CPU control unit design: hardwired and micro-programmed design approaches, Memory system design: semiconductor memory technologies, Memory Organization- Memory Hierarchy, Main Memory, Auxiliary memory, Associate Memory, Cache Memory.

Peripheral devices and their characteristics: I/O subsystems, I/O device interface, I/O transfers–program controlled, Asynchronous data transfer, Modes of Transfer, interrupt driven and DMA,

Privileged and non-privileged instructions, software interrupts and exceptions. Programs and processes–role of interrupts in process state transitions, I/O device interfaces – SCII, USB

Module-IV: (07 Hrs.)

Reduced Instruction Set Computer: CISC Characteristics, RISC Characteristics.

Pipeline and Vector Processing: Pipelining: Basic concepts of pipelining, throughput and speedup, pipeline hazards. Vector Processing, Array Processor.

Multi Processors: Characteristics of Multiprocessors, Interconnection Structures, Inter-processor arbitration, Inter-processor communication and synchronization, Cores, and Hyper-Threading ,Cache Coherence.

Module-V: (08 Hrs.)

Memory organization: Memory interleaving, concept of hierarchical memory organization, cache memory, cache size vs. block size, mapping functions, replacement algorithms, write policies.

Books:

1. "Computer Organization and Embedded Systems", 6th Edition by CarlHamacher, McGraw Hill Higher Education.
2. "Computer Organization and Architecture: Designing for Performance", 10th Edition by William Stallings, Pearson Education.
3. "Computer Architecture and Organization", 3rd Edition by John P. Hayes, WCB/McGraw-Hill
4. "Computer Organization and Design: The Hardware/Software Interface", 5th Edition by David A. Patterson and John L. Hennessy, Elsevier.

Course outcomes

1. Draw the functional block diagram of a single bus architecture of a computer and describe the function of the instruction execution cycle, RTL interpretation of instructions, addressing modes, instruction set.
2. Write assembly language program for specified microprocessor for computing 16-bit multiplication, division and I/O device interface (ADC, Control circuit, serial port communication).
3. Write a flowchart for Concurrent access to memory and cache coherency in Parallel Processors and describe the process.
4. Given a CPU organization and instruction, design a memory module and analyze its operation by interfacing with the CPU.
5. Given a CPU organization, assess its performance, and apply design techniques to enhance performance using pipelining, parallelism and RISC methodology